What is claimed is:

1. A data storage system comprising:

a plurality of memory subarrays, each subarray comprising a plurality of memory cells and a plurality of subarray bitlines, each memory cell being configurable to store one of a plurality of signal levels and being coupled to one of said subarray bitlines;

a plurality of local sense amplifiers, each of said plurality of local sense amplifiers being coupled to a corresponding one of said plurality of memory subarrays and being selectively coupled to said subarray bitlines and said memory subarray;

a plurality of global bitlines, each local sense amplifier being coupled to one of said plurality of global bitlines; and

a plurality of global sense amplifiers, each global sense amplifier being coupled to a group of said global bitlines.

2. The data storage system of claim 1 wherein the plurality of memory cells are multilevel cells.

3. The data storage system of claim 1, wherein said global sense amplifier comprises a common source stage and the local sense amplifier comprises a source follower stage.

4. The data storage system of claim 1,

wherein said local sense amplifier comprises:

an NMOS transistor including a first terminal coupled to a corresponding global bitline, including a second terminal spaced apart from said first terminal with a channel therebetween and coupled to a ground terminal, and including a gate for controlling current in said channel and coupled to a node that is selectively coupled to one of said group of subarray bitlines,

a current source coupled between said gate of said NMOS transistor and said ground terminal; and

wherein said global sense amplifier comprises:

a PMOS transistor including a first terminal coupled to a power terminal, including a second terminal spaced apart from said first terminal with a channel therebetween and selectively coupled to one of said group of global bitlines, and including a gate for controlling current in said channel and coupled to said second terminal, and

a comparator having a first terminal coupled to the second terminal of the PMOS transistor, having a second terminal coupled to a reference voltage terminal, and having an output.

5. The data storage system of claim 1, wherein said global sense amplifier comprises a source follower stage, and the local sense amplifier comprises a source follower stage and includes a PMOS transistor.

6. The data storage system of claim 5 wherein said PMOS transistor operates as part of the source follower stage of the global sense amplifier.

7. The data storage system of claim 1,

wherein said local sense amplifier comprises:

a PMOS transistor including a first terminal coupled to a corresponding global bitline, including a second terminal spaced apart from said first terminal with a channel therebetween and coupled to a ground terminal, and including a gate for controlling current in said channel and coupled to a node that is selectively coupled to one of said group of subarray bitlines,

a current source coupled between said gate of said NMOS transistor and said ground terminal; and

wherein said global sense amplifier comprises:

a current source including a first terminal coupled to a power terminal and including a second terminal coupled to the global bit line, and

a comparator having a first terminal coupled to the second terminal of the current source, having a second terminal coupled to a reference voltage terminal, and having an output.

8. The data storage system of claim 1, wherein said global sense amplifier comprises a source follower stage, and the local sense amplifier comprises a source follower stage and includes an NMOS transistor.

9. The data storage system of claim 8 wherein said NMOS transistor operates as part of the source follower stage of the global sense amplifier.

10. The data storage system of claim 1,

wherein said local sense amplifier comprises:

an NMOS transistor including a first terminal coupled to a corresponding global bitline, including a second terminal spaced apart from said first terminal with a channel therebetween and coupled to a power terminal, and including a gate for controlling current in said channel and coupled to a node that is selectively coupled to one of said group of subarray bitlines,

a current source coupled between said gate of said NMOS transistor and said ground terminal; and

wherein said global sense amplifier comprises:

a current source including a first terminal coupled to a ground terminal and including a second terminal selectively coupled to one of said group of global bitlines and

a comparator having a first terminal coupled to the second terminal of said current source, having a second terminal coupled to a reference voltage terminal, and having an output.

11. The storage system of claim 1, wherein said global sense amplifier comprises a common source stage, and the local sense amplifier comprises a common source stage.

12. The data storage system of claim 1, wherein said global sense amplifier comprises a source follower stage, and the local sense amplifier comprises a common source stage.

13. The data storage system of claim 1, wherein said global sense amplifier comprises:

a comparator having first and second inputs, and having first and second outputs;

a first capacitor having a first terminal coupled to the first input of the comparator and having a second terminal selectively coupled to a reference voltage terminal; and

a second capacitor having a first terminal coupled to the second input terminal of the comparator and having a second terminal selectively coupled to the reference voltage terminal and a cell voltage terminal.

14. The data storage system of claim 13 further comprising a first switch to selectively couple the first input terminal of the comparator to the first output terminal of the comparator and further comprising a second switch for connecting the second input terminal of the comparator to the second output terminal of the comparator.

15. The data storage system of claim 14 wherein the second terminals of the first and second capacitors are coupled to the reference voltage terminal and the first and second inputs of the comparator are coupled to the first and second outputs, respectively, of the comparator.

16. The data storage system of claim 14 wherein the first terminals of the first and second capacitors are coupled to a bias voltage.

17. The data storage system of claim 13 wherein the first terminals of the first and second capacitors are coupled to each other.

18. The data storage system of claim 1, wherein said sense amplifier comprises a comparator including:

a first transistor of a first type including a first terminal coupled to a power terminal, including a second terminal spaced apart from said first terminal with a channel therebetween and coupled to an output terminal, and including a gate for controlling current in said channel and coupled;

a second transistor of the first type including a first terminal coupled to the power terminal, including a second terminal spaced apart from said first terminal with a channel therebetween and coupled to the gate of the first transistor of the first type, and including a gate

for controlling current in said channel and coupled to the second terminal of the first transistor of the first type;

a first transistor of a second type including a first terminal coupled to the second terminal of the first transistor of the first type, including a second terminal spaced apart from said first terminal with a channel therebetween, and including a gate for controlling current in said channel;

a second transistor of the second type including a first terminal coupled to the second terminal of the second transistor of the first type, including a second terminal spaced apart from said first terminal with a channel therebetween and coupled to the second terminal of the first transistor of the first type, and including a gate for controlling current in said channel;

a third transistor of the second type including a first terminal coupled to the common node formed of the second terminals of the first and second transistors of the second type, including a second terminal spaced apart from said first terminal with a channel therebetween and coupled to a ground terminal, and including a gate for controlling current in said channel;

a first capacitor including a first terminal coupled to the gate of the first transistor of the second type and including a second terminal coupled to selectively coupled to a reference voltage or to a global bitline;

a second capacitor including a first terminal coupled to the gate of the second transistor of the second type and including a second terminal coupled to selectively coupled to the reference voltage;

a fourth transistor of the second type including a first terminal coupled to the second terminal of the first transistor of the first type, including a second terminal spaced apart from said first terminal with a channel therebetween, and including a gate for controlling current in said channel and coupled to the first terminal of the second transistor of the second type;

a fifth transistor of the second type including a first terminal coupled to gate of the fourth transistor of the second type, including a second terminal spaced apart from said first terminal with a channel therebetween and coupled to the second terminal of the fourth transistor of the second type, and including a gate for controlling current in said channel and coupled to a first terminal of the fourth transistor of the second type; and

a sixth transistor of the second type including a first terminal coupled to the second terminal of the fourth transistor of the second type, including a second terminal spaced apart

from said first terminal with a channel therebetween and coupled to the ground terminal, and including a gate for controlling current in said channel.

19. The data storage system of claim 18, wherein the comparator further includes:

an equalization circuit coupling the second terminals of the first and second transistors of the first type to equalize the voltages thereof.

20. The data storage system of claim 19 further comprising a first autozero circuit to equalize the second terminals of the first and second capacitors.

21. The data storage system of claim 19 further comprising a second auto zero circuit to equalize the first terminals of the first and second capacitors to the second terminals of the respective first and second transistors of the first type.

22. An integrated circuit data storage system comprising:

a plurality of memory cells, each memory cell being configurable to store one of a plurality of signal levels;

a plurality of local bitlines, each memory cell being coupled to one of said subarray bitlines;

a plurality of global bitlines;

a plurality of local sense amplifiers, each of said plurality of local sense amplifiers being coupled to a corresponding group of ones of said plurality of memory cells and being selectively coupled to said local bitlines, each local sense amplifier being coupled to one of said plurality of global bitlines;

a plurality of global sense amplifiers, each global sense amplifier being coupled to a group of said global bitlines;

a decoding circuit coupled to the plurality of memory cells and configured to generate a first and a second control signal based on a set of input data bits; and

a supply source operatively coupled to selected ones of the plurality of memory cells based on the first control signal from the decoding circuit, the supply source configured to provide programming signals based on the second control signal, and

wherein the selected memory cells are programmed in accordance with the programming signals from the supply source.

23. The device of claim 22, wherein the plurality of memory cells are arranged into a plurality of memory arrays, each memory array including P rows by Q columns of memory cells, and said local bit lines are coupled to subsets of the Q columns of memory cells.

24. The device of claim 23, wherein each memory array is partitioned into a plurality of memory segments, each memory segment including R rows by S columns of memory cells, wherein each memory segment is further partitioned into a plurality of memory blocks, each memory block including X rows by Y columns of memory cells, each of said local sense amplifiers being coupled to a corresponding one of said memory blocks.

25. The device of claim 22, wherein the local bit lines couple to the global bit lines via a first set of transistors.

26. The device of claim 25, wherein the transistors in the first set are enabled by associated bit line select lines.

27. The memory system of claim 22, wherein the memory unit further includes

at least one redundant array of memory cells, each redundant array configurable to substitute for a subset of the plurality of memory cells in the memory unit, a local sense amplifier being coupled to said redundant array.

28. An integrated circuit memory device having a semiconductor substrate, said memory device comprising:

a plurality of memory cells at a surface of said semiconductor substrate;

a decoding circuit configured to generate a set of control signals based on an address;

a plurality of bit lines, each bit line interconnecting a subset of the plurality of memory cells formed in a memory array, each bit formed as a main metal bit line and a plurality of segmented metal bit lines, the main metal bit line traversing a length of the memory array, the

segmented metal bit lines each traversing a portion of the length of the memory array, selectively connected to the main bit line responsive to the control signals from the decoding circuit and connected to semiconductor substrate regions of the memory cells alone the portion of the length of the memory array, the segmented metal bit lines passing over the semiconductor substrate and the main bit line passing over the segmented metal bit lines so that capacitance of each bit line is reduced;

a plurality of local sense amplifiers, each of said plurality of local sense amplifiers being coupled to a corresponding one of subsets of memory cells and being selectively coupled to said segmented bit lines and the bit lines; and

a plurality of global sense amplifiers, each global sense amplifier being coupled to a group of said bit lines.

29. The device of claim 28, wherein the plurality of memory cells are arranged into a plurality of memory arrays, each memory array including P rows by Q columns of memory cells.

30. The device of claim 29, wherein each memory array is partitioned into a plurality of memory segments, each memory segment including R rows by S columns of memory cells, wherein each memory segment is further partitioned into a plurality of memory blocks, each memory block including X rows by Y columns of memory cells.

31. The device of claim 30, wherein each segmented bit line couples to memory cells in a column of a memory block.

32. The device of claim 30, wherein each main bit line couples to segmented bit lines associated with a column of a memory segment.

33. The device of claim 28, wherein the segmented bit lines couple to the main bit lines via a first set of transistors.

34. A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, each memory cell is configurable to store one of 2^N values, where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells;

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells;

a plurality of local sense amplifiers, each of said plurality of local sense amplifiers being coupled to a corresponding subset of said plurality of memory cells and being selectively coupled to said bit lines;

a plurality of global bit lines, each local sense amplifier being coupled to one of said plurality of global bitlines; and

a plurality of global sense amplifiers, each global sense amplifier being coupled to a group of said global bitlines and said reference array to generate an output signal indicative of the comparison between a voltage detected in a selected memory cell and a reference signal.

35. A data storage system comprising:

a plurality of memory arrays,

each memory array comprising:

a plurality of memory subarrays, each memory subarray including a plurality of memory cells;

a plurality of local sense amplifiers, each local sense amplifier being coupled to a corresponding one of the plurality of memory subarrays, the local sense amplifier reading the contents of memory cells within the corresponding memory subarray, and

a plurality of global sense amplifiers, each global sense amplifier being coupled to a group of said plurality of local sense amplifiers.

36. The data storage system of claim 35 wherein the plurality of memory arrays are arranged in rows and columns.

37. The data storage system of claim 35 wherein the plurality of memory subarrays are arranged in rows and columns.

38. A data storage system comprising:

a plurality of memory arrays, each memory array comprising:

a plurality of memory subarrays, each memory subarray including a plurality of memory cells,

a plurality of local sense amplifiers, each local sense amplifier being disposed adjacent to and coupled to a group of said memory subarrays, the local sense amplifier reading the contents of the memory cells within the corresponding group of memory subarrays, and

a plurality of global sense amplifiers, each global sense amplifier being coupled to a group of said local sense amplifiers.

39. The data storage system of claim 38 wherein the plurality of memory arrays are arranged in rows and columns.

40. The data storage system of claim 38 wherein the plurality of memory subarrays are arranged in rows and columns.

41. A data storage system comprising:

a reference array including a plurality of reference cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, each reference cell is configurable to store one of 2^N values, where N is at least two or greater;

a plurality of local sense amplifiers, each of said plurality of local sense amplifiers being coupled to a corresponding subset of said plurality of reference cells and being selectively coupled to said bitlines;

a plurality of global bitlines, each local sense amplifier being coupled to one of said plurality of global bitlines; and

a plurality of global sense amplifiers, each global sense amplifier being coupled to a group of said global bitlines to generate an output signal indicative of a reference signal corresponding to the selected reference cell.

42. A data storage system comprising:

a plurality of memory subarrays, each memory subarray comprising a plurality of memory cells, each memory cell being configurable to store one of a plurality of signal levels; and

a plurality of sense amplifiers, each sense amplifier being selectively coupled to a corresponding subarray to capacitively sense content of a memory cell.

43. A data storage system comprising:

a plurality of memory subarrays, each subarray comprising a plurality of memory cells, each memory cell being configurable to store one of a plurality of signal levels;

a plurality of local sense amplifiers, each of said plurality of local sense amplifiers being selectively coupled to a corresponding one of said plurality of memory subarrays; and

a plurality of global sense amplifiers, each global sense amplifier being selectively coupled to a group of said local sense amplifiers to capacitively sense a voltage on said group of local sense amplifiers.

44. The data storage system of claim 43, wherein said global sense amplifier comprises:

a comparator having first and second inputs, and having first and second outputs;

a first capacitor having a first terminal coupled to the first input of the comparator and having a second terminal selectively coupled to a reference voltage terminal; and

a second capacitor having a first terminal coupled to the second input terminal of the comparator and having a second terminal selectively coupled to the reference voltage terminal and a cell voltage terminal.

45. A data storage system comprising:

a plurality of memory subarrays, each memory subarray comprising a plurality of memory cells, each memory cell being configurable to store one of a plurality of signal levels; and

a plurality of sense amplifiers, each sense amplifier being selectively coupled to a memory subarray to sense with autozero content of a memory cell.

46. A data storage system comprising:

a plurality of memory subarrays, each subarray comprising a plurality of memory cells, each memory cell being configurable to store one of a plurality of signal levels;

a plurality of local sense amplifiers, each of said plurality of local sense amplifiers being selectively coupled to a corresponding one of said plurality of memory subarrays; and

a plurality of global sense amplifiers, each global sense amplifier having a first input coupled to a group of said local sense amplifiers, having a second input coupled to a reference voltage terminal, having first and second outputs for providing first and second output signals in response to signals applied to said first and second inputs, and including a circuit for coupling said first input to said first output and coupling said second input to said second output in response to an autozero signal.

47. The data storage system of claim 46 wherein said circuit comprises:

a first switch to selectively couple the first input of the sense amplifier to the first output of the global sense amplifier; and

a second switch for connecting the second input of the global sense amplifier to the second output of the global sense amplifier.

48. A data storage system comprising:

a plurality of memory subarrays, each memory subarray comprising a plurality of memory cells, each memory cell being configurable to store one of a plurality of signal levels; and

a plurality of sense amplifiers, each sense amplifier being selectively coupled to a memory subarray to sense with substantially constant input common mode range content of a memory cell.

49. A data storage system comprising:

a plurality of memory subarrays, each subarray comprising a plurality of memory cells, each memory cell being configurable to store one of a plurality of signal levels;

a plurality of local sense amplifiers, each of said plurality of local sense amplifiers being selectively coupled to a corresponding one of said plurality of memory subarrays; and

a plurality of global sense amplifiers, each global sense amplifier being coupled to a group of said local sense amplifiers to provide an input range to the global sense amplifier substantially independent of a state of a selected memory cell.

50. A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, each memory cell is configurable to store one of 2^N values, where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells;

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells, the reference signals being stored in a real time relationship to receiving programming signals corresponding to said reference signals;

a plurality of local sense amplifiers, each of said plurality of local sense amplifiers being coupled to a corresponding subset of said plurality of memory cells and being selectively coupled to said bit lines;

a plurality of global bit lines, each local sense amplifier being coupled to one of said plurality of global bitlines; and

a plurality of global sense amplifiers, each global sense amplifier being coupled to a group of said global bitlines and said reference array to generate an output signal indicative of the comparison between a voltage detected in a selected memory cell and a reference signal.

51. The data storage system of claim 50 wherein the global sense amplifier capacitively detects a voltage on one of said global bitlines and capacitively detects one of said reference signals and generates an output signal indicative of the comparison between said detected voltage and a selected reference cell and said detected reference signal.

52. The data storage system of claim 50 wherein the global sense amplifier includes a circuit for coupling inputs of the global sense amplifier to the output signal in response to an autozero signal.

53. A data storage system comprising:

a plurality of reference memory subarrays, each reference memory subarray comprising a plurality of reference memory cells, each memory cell being configurable to store one of a plurality of reference signal levels; and

a plurality of reference sense amplifiers, each reference sense amplifier being selectively coupled to a corresponding subarray to capacitively sense content of a memory cell.

54. A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, each memory cell is configurable to store one of 2^N values, where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells;

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells, the reference signals being stored in a real time relationship to receiving programming signals corresponding to said reference signals;

a plurality of local sense amplifiers, each of said plurality of local sense amplifiers being coupled to a corresponding subset of said plurality of memory cells and being selectively coupled to said bit lines;

a plurality of global bit lines, each local sense amplifier being coupled to one of said plurality of global bitlines; and

a plurality of global sense amplifiers, each global sense amplifier being coupled to a group of said global bitlines to capacitively detect a voltage on one of said global bitlines and to said reference array to capacitively detect one of said reference signals, and to generate an output signal indicative of the comparison between said detected voltage in a selected memory cell and said detected reference signal.

55. A data storage system comprising:

a plurality of reference memory subarrays, each reference memory subarray comprising a plurality of reference memory cells, each reference memory cell being configurable to store one of a plurality of reference signal levels; and

a plurality of reference sense amplifiers, each sense reference amplifier being selectively coupled to a reference memory subarray to sense with autozero content of a reference memory cell.

56. A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, each memory cell is configurable to store one of 2^N values, where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells;

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells, the reference signals being stored in a real time relationship to receiving programming signals corresponding to said reference signals;

a plurality of local sense amplifiers, each of said plurality of local sense amplifiers being coupled to a corresponding subset of said plurality of memory cells and being selectively coupled to said bit lines;

a plurality of global bit lines, each local sense amplifier being coupled to one of said plurality of global bitlines; and

a plurality of global sense amplifiers, each global sense amplifier being coupled to a group of said global bitlines to capacitively detect a voltage on one of said global bitlines and said reference array to capacitively detect one of said reference signals to generate an output signal indicative of the comparison between said detected voltage in a selected memory cell and said detected reference signal, and including a circuit to equalize inputs and the output of the global sense amplifier in response to an autozero signal.

57. A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, each memory cell is configurable to store one of 2^N values, where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells;

a plurality of local sense amplifiers, each of said plurality of local sense amplifiers being coupled to a corresponding subset of said plurality of memory cells and being selectively coupled to said bit lines;

a plurality of global bit lines, each local sense amplifier being coupled to one of said plurality of global bitlines;

a plurality of global sense amplifiers, each global sense amplifier being coupled to a group of said global bitlines to generate an output signal indicative of the comparison between a voltage detected in a selected memory cell and a plurality of reference signals detected on a reference signal terminal; and

a circuit to compare the output signal from one of said global sense amplifiers corresponding to a selected memory cell and said detected reference signal to verify contents of said selected memory cell and programming said selected memory cell in the event the comparison indicates content of said selected memory cell does not match said one of said detected reference signals.

58. The data storage system of claim 57 further comprising a reference array operatively coupled to the memory arrays and configurable to provide stored reference signals used for programming and reading the selected ones of the plurality of memory cells, the stored reference signals corresponding to said detected plurality of reference signals.

59. A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, each memory cell is configurable to store one of 2^N values, where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells;

a plurality of local sense amplifiers, each of said plurality of local sense amplifiers being coupled to a corresponding subset of said plurality of memory cells and being selectively coupled to said bit lines;

a plurality of global bit lines, each local sense amplifier being coupled to one of said plurality of global bitlines;

a plurality of global sense amplifiers, each global sense amplifier being coupled to a group of said global bitlines to capacitively detect a voltage on one of said global bitlines and to capacitively detect one of a plurality of reference signals to generate an output signal indicative of the comparison between said detected voltage in a selected memory cell and said detected reference signal; and

a circuit to compare the output signal from one of said global sense amplifiers corresponding to a selected memory cell and said detected reference signal to verify contents of said selected memory cell and programming said selected memory cell in the event the comparison indicates content of said selected memory cell does not match said one of said detected reference signals.

60. The data storage system of claim 59 further comprising a reference array operatively coupled to the memory arrays and configurable to provide stored reference signals used for programming and reading the selected ones of the plurality of memory cells, the stored reference signals corresponding to said detected plurality of reference signals.

61. A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, each memory cell is configurable to store one of 2^N values, where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells;

a plurality of local sense amplifiers, each of said plurality of local sense amplifiers being coupled to a corresponding subset of said plurality of memory cells and being selectively coupled to said bit lines;

a plurality of global bit lines, each local sense amplifier being coupled to one of said plurality of global bitlines;

a plurality of global sense amplifiers, each global sense amplifier being coupled to a group of said global bitlines to generate an output signal indicative of the comparison between a voltage detected in a selected memory cell and one of a plurality of reference signals, and including a circuit to equalize inputs and the output of the global sense amplifier in response to an autozero signal; and

a circuit to compare the output signal from one of said global sense amplifiers corresponding to a selected memory cell and said detected reference signals from said reference array to verify contents of said selected memory cell and programming said selected memory cell in the event the comparison indicates content of said selected memory cell does not match said detected reference signals.

62. The data storage system of claim 61 further comprising a reference array operatively coupled to the memory arrays and configurable to provide stored reference signals used for programming and reading the selected ones of the plurality of memory cells, the stored reference signals corresponding to said detected plurality of reference signals.

63. A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, each memory cell is configurable to store one of 2^N values, where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells;

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells;

a plurality of local sense amplifiers, each of said plurality of local sense amplifiers being coupled to a corresponding subset of said plurality of memory cells;

a plurality of global sense amplifiers, each global sense amplifier being coupled to a group of local sense amplifiers and said reference array to generate an output signal indicative of the comparison between a voltage detected in a selected memory cell and a reference signal; and

a circuit to compare the output signal from one of said global sense amplifiers corresponding to a selected memory cell and one of said reference signals from said reference array and determining whether said output signal is within a predetermined relationship of said one of said reference signals during a programming, erase or reading of said selected memory cell and setting a flag to indicate whether a predetermined relationship is determined.

64. A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, each memory cell is configurable to store one of 2^N values, where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells;

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells;

a plurality of local sense amplifiers, each of said plurality of local sense amplifiers being coupled to a corresponding subset of said plurality of memory cells and being selectively coupled to said bit lines;

a plurality of global bit lines, each local sense amplifier being coupled to one of said plurality of global bitlines;

a plurality of global sense amplifiers, each global sense amplifier being coupled to a group of said global bitlines and said reference array to generate an output signal indicative of the comparison between a voltage detected in a selected memory cell and a reference signal; and

a circuit to compare the output signal from one of said global sense amplifiers corresponding to a selected memory cell and one of said reference signals from said reference array and determining whether said output signal is within a predetermined relationship of said one of said reference signals during a programming, erase or reading of said selected memory cell and setting a flag to indicate whether a predetermined relationship is determined.

65. The data storage system of claim 64 wherein said circuit reprograms said selected memory cell in the event the circuit determines said output signals within a margin of said one of said reference signals.

66. The data storage system of claim 65, wherein said circuit further compares the output signal from said one of said global sense amplifiers corresponding to said selected memory cell and another one of said reference signals from said reference array in determining whether said output signal is within another margin of said another one of said reference signals.

67. The data storage system of claim 66 wherein said circuit reprograms said selected memory cell in the event the circuit determines said output signals within a margin of said one of said reference signals.

68. A data storage system comprising:

a plurality of memory subarrays, each subarray comprising a plurality of memory cells, each memory cell being configurable to store one of a plurality of signal levels;

a sense amplifier capacitively sense a voltage of a selected memory cell;

a circuit to compare an output signal from said sense amplifiers corresponding to a selected memory cell and one of a plurality of reference signals and to determine whether said output signal is within a predetermined relationship of said one of said reference signals during a programming, erase or reading of said selected memory cell and setting a flag to indicate whether a predetermined relationship is determined.

69. A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, each memory cell is configurable to store one of 2^N values, where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells;

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells;

a plurality of local sense amplifiers, each of said plurality of local sense amplifiers being coupled to a corresponding subset of said plurality of memory cells and being selectively coupled to said bit lines;

a plurality of global bit lines, each local sense amplifier being coupled to one of said plurality of global bitlines;

a plurality of global sense amplifiers, each global sense amplifier being coupled to a group of said global bitlines to capacitively detect a voltage on one of said global bitlines and said reference array to capacitively detect one of said reference signals to generate an output signal indicative of the comparison between said detected voltage in a selected memory cell and a reference signal; and

a circuit to compare the output signal from one of said global sense amplifiers corresponding to a selected memory cell and one of said reference signals from said reference array and determining whether said output signal is within a predetermined relationship of said one of said reference signals during a programming, erase or reading of said selected memory cell and setting a flag to indicate whether a predetermined relationship is determined.

70. A data storage system comprising:

a plurality of memory subarrays, each subarray comprising a plurality of memory cells, each memory cell being configurable to store one of a plurality of signal levels;

a sense amplifier to sense a voltage of a selected memory cell and auto zero an input and an output of said sense amplifier before sensing said voltage;

a circuit to compare an output signal from said sense amplifiers corresponding to a selected memory cell and one of a plurality of reference signals and to determine whether said output signal is within a predetermined relationship of said one of said reference signals during a programming, erase or reading of said selected memory cell and setting a flag to indicate whether a predetermined relationship is determined.

71. A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, each memory cell is configurable to store one of 2^N values, where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells;

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells;

a plurality of local sense amplifiers, each of said plurality of local sense amplifiers being coupled to a corresponding subset of said plurality of memory cells and being selectively coupled to said bit lines;

a plurality of global bit lines, each local sense amplifier being coupled to one of said plurality of global bitlines;

a plurality of global sense amplifiers, each global sense amplifier being coupled to a group of said global bitlines and said reference array to generate an output signal indicative of the comparison between a voltage detected in a selected memory cell and a reference signal, and including a circuit to equalize inputs and the output of the global sense amplifier in response to an autozero signal; and

a circuit to compare the output signal from one of said global sense amplifiers corresponding to a selected memory cell and one of said reference signals from said reference array and determining whether said output signal is within a predetermined relationship of said one of said reference signals during a programming, erase or reading of said selected memory cell and setting a flag to indicate whether a predetermined relationship is determined.

72. The data storage system of claim 71 wherein said circuit reprograms said selected memory cell in the event the circuit determines said output signals are within a margin of said one of said reference signals.

73. The data storage system of claim 71, wherein said circuit further compares the output signal from said one of said global sense amplifiers corresponding to said selected memory cell

and another one of said reference signals from said reference array to determine whether said output signal is within another margin of said another one of said reference signals.

74. The data storage system of claim 73 wherein said circuit reprograms said selected memory cell in the event the circuit determines said output signal is within a margin of said one of said reference signals.

75. A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, each memory cell is configurable to store one of 2^N values, where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells;

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells;

a plurality of local sense amplifiers, each of said plurality of local sense amplifiers being coupled to a corresponding subset of said plurality of memory cells and being selectively coupled to said bit lines;

a plurality of global bit lines, each local sense amplifier being coupled to one of said plurality of global bitlines;

a plurality of global sense amplifiers, each global sense amplifier being coupled to a group of said global bitlines and said reference array to generate an output signal indicative of the comparison between a voltage detected in a selected memory cell and a reference signal; and

a circuit to compare the output signal from one of said global sense amplifiers corresponding to a selected memory cell and one of said reference signals from said reference array and determining whether said output signal is within a predetermined relationship of said one of said reference signals during a programming, erase or reading of said selected memory cell and setting a flag to indicate whether a predetermined relationship is determined.

76. A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, each memory cell is configurable to store one of 2^N values, where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells;

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells;

a plurality of local sense amplifiers, each of said plurality of local sense amplifiers being coupled to a corresponding subset of said plurality of memory cells and being selectively coupled to said bit lines;

a plurality of global bit lines, each local sense amplifier being coupled to one of said plurality of global bitlines;

a plurality of global sense amplifiers, each global sense amplifier being coupled to a group of said global bitlines to capacitively detect a voltage on one of said global bitlines and said reference array to capacitively detect one of said reference signals to generate an output signal indicative of the comparison between said detected voltage in a selected memory cell and a reference signal; and

a circuit to compare the output signal from one of said global sense amplifiers corresponding to a selected memory cell and one of said reference signals from said reference array and determining whether said output signal is within a predetermined relationship of said one of said reference signals during programming, erasing or reading of said selected memory cell and setting a flag to indicate whether a predetermined relationship is determined.

77. A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, each memory cell is configurable to store one of 2^N values, where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells;

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells;

a plurality of local sense amplifiers, each of said plurality of local sense amplifiers being coupled to a corresponding subset of said plurality of memory cells and being selectively coupled to said bit lines;

a plurality of global bit lines, each local sense amplifier being coupled to one of said plurality of global bitlines;

a plurality of global sense amplifiers, each global sense amplifier being coupled to a group of said global bitlines and said reference array to generate an output signal indicative of the comparison between a voltage detected in a selected memory cell and a reference signal and including a circuit to equalize inputs and the output of the global sense amplifier in response to an autozero signal; and

a circuit to compare the output signal from one of said global sense amplifiers corresponding to a selected memory cell and one of said reference signals from said reference array and determining whether said output signal is within a predetermined relationship of said one of said reference signals during a programming, erase or reading of said selected memory cell and setting a flag to indicate whether a predetermined relationship is determined.

78. A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, each memory cell is configurable to store one of 2^N values, where N is two or greater, the memory cell being programmed in response to a shaped program pulse applied to said at least one common line;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells;

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells;

a plurality of local sense amplifiers, each of said plurality of local sense amplifiers being coupled to a corresponding subset of said plurality of memory cells and being selectively coupled to said bit lines;

a plurality of global bit lines, each local sense amplifier being coupled to one of said plurality of global bitlines; and

a plurality of global sense amplifiers, each global sense amplifier being coupled to a group of said global bitlines and said reference array to generate an output signal indicative of the comparison between a voltage detected in a selected memory cell and a reference signal.

79. The data storage system of claim 78 wherein said shaped program pulse has a two-step ramp rate.

80. A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, each memory cell is configurable to store one of 2^N values, where N is two or greater, the memory cell being programmed in response to a shaped program pulse applied to said at least one common line;

a plurality of sense amplifiers, each sense amplifier being selectively coupled to a corresponding subarray to capacitively sense content of a memory cell.

81. A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, each memory cell is configurable to store one of 2^N values, where N is two or greater, the memory cell being programmed in response to a shaped program pulse applied to said at least one common line;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells;

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells;

a plurality of local sense amplifiers, each of said plurality of local sense amplifiers being coupled to a corresponding subset of said plurality of memory cells and being selectively coupled to said bit lines;

a plurality of global bit lines, each local sense amplifier being coupled to one of said plurality of global bitlines; and

a plurality of global sense amplifiers, each global sense amplifier being coupled to a group of said global bitlines to capacitively detect a voltage on one of said global bitlines and said reference array to capacitively detect one of said reference signals to generate an output signal indicative of the comparison between said detected voltage in a selected memory cell and a reference signal.

82. The data storage system of claim 81, wherein the shaped program pulse has a two-step ramp rate.

83. The data storage system of claim 81 wherein the ramp rate is programmable.

84. A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, each memory cell is configurable to store one of 2^N values, where N is two or greater, the memory cell being programmed in response to a shaped program pulse applied to said at least one common line; and

a plurality of sense amplifiers, each sense amplifier being selectively coupled to a memory subarray to sense with autozero content of a memory cell.

85. A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, each memory cell is configurable to store one of 2^N values, where N is two or greater, the memory cell being programmed in response to a shaped program pulse applied to said at least one common line;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells;

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells;

a plurality of local sense amplifiers, each of said plurality of local sense amplifiers being coupled to a corresponding subset of said plurality of memory cells and being selectively coupled to said bit lines;

a plurality of global bit lines, each local sense amplifier being coupled to one of said plurality of global bitlines; and

a plurality of global sense amplifiers, each global sense amplifier being coupled to a group of said global bitlines and said reference array to generate an output signal indicative of the comparison between a voltage detected in a selected memory cell and a reference signal and including a circuit to equalize inputs and the output of the global sense amplifier in response to an autozero signal.

86. The data storage system of claim 85, wherein the shaped program pulse has a two-step ramp rate.

87. The data storage system of claim 85, wherein the ramp rate is programmable.

88. A method of programming a multilevel memory cell, the method comprising:

determine whether margin of read said memory cell matches a certain criteria;

setting a program fail flag in the event the margin does not match said criteria;

perform binary search to determine data corresponding to content of read memory cell; and

allowing access to said memory cell.

89. A method comprising:

Read a fuse non-volatile memory location for configuration data in response to a page read command;

Store said configuration data in a volatile memory location; and

Using the configuration data to initiate a page read sequence for a memory.

90. A method comprising:

Read a fuse non-volatile memory location for configuration data in response to a page program command;

Store said configuration data in a volatile memory location; and

Using the configuration data to initiate a page programming sequence for a memory.

91. A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, each memory cell is configurable to store one of 2^N values, where N is two or greater; and

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells, and provide a first one of said bias signals to one of the plurality of memory arrays to select ones of the plurality of memory cells therein and provide a second one of said bias signals to another one of the plurality of memory arrays to enable reading of said another one of the plurality of memory arrays while reading said one of the plurality of memory arrays.

92. The data storage system of claim 91 further comprising:

a plurality of local sense amplifiers, each of said plurality of local sense amplifiers being coupled to a corresponding memory array and coupled through bit lines to memory cells in said corresponding memory array; and

a plurality of global sense amplifiers, each global sense amplifier being coupled to a group of said plurality of local sense amplifiers to generate an output signal indicative of the content of selected memory cells.

93. The data storage system of claim 92 wherein said at least one memory decoder selectively enabling two of said local sense amplifiers coupled to a corresponding global sense amplifier while selectively coupling an output of one of the local sense amplifiers to said corresponding global sense amplifier and enabling another one of said local sense amplifiers

coupled to said corresponding global sense amplifier while selectively coupling an output of another one of said two local sense amplifiers.

94. The data storage system of claim 92 wherein each global sense amplifier is selectively coupled to a group of said local sense amplifiers to capacitively sense a voltage on said group of local sense amplifiers.

95. The data storage system of claim 92 wherein each global sense amplifier is selectively coupled to a group of said local sense amplifiers to capacitively sense a voltage on said group of local sense amplifiers.

96. The data storage system of claim 92 wherein each global sense amplifier auto zeros an input and output to zero out offset of the global sense amplifier.

97. A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, each memory cell is configurable to store one of 2^N values, where N is two or greater; and

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells, and provide a first one of said bias signals to one of the plurality of memory arrays to select ones of the plurality of memory cells therein and provide a second one of said bias signals to another one of the plurality of memory arrays to enable writing of said another one of the plurality of memory arrays while reading said one of the plurality of memory arrays.

98. The data storage system of claim 97 further comprising:

a plurality of local sense amplifiers, each of said plurality of local sense amplifiers being coupled to a corresponding memory array and coupled through bit lines to memory cells in said corresponding memory array; and

a plurality of global sense amplifiers, each global sense amplifier being coupled to a group of said plurality of local sense amplifiers to generate an output signal indicative of the content of selected memory cells.

99. The data storage system of claim 98 wherein said at least one memory decoder selectively enabling two of said local sense amplifiers coupled to a corresponding global sense amplifier while selectively coupling an output of one of the local sense amplifiers to said corresponding global sense amplifier and enabling another one of said local sense amplifiers coupled to said corresponding global sense amplifier while selectively coupling an output of another one of said two local sense amplifiers.

100. The data storage system of claim 99 wherein each global sense amplifier is selectively coupled to a group of said local sense amplifiers to capacitively sense a voltage on said group of local sense amplifiers.

101. The data storage system of claim 98 wherein each global sense amplifier is selectively coupled to a group of said local sense amplifiers to capacitively sense a voltage on said group of local sense amplifiers.

102. The data storage system of claim 98 wherein each global sense amplifier auto zeros an input and output to zero out offset of the global sense amplifier.

103. A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, each memory cell is configurable to store one of 2^N values, where N is two or greater; and

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells, and provide a first one of said bias signals to one of the plurality of memory arrays to select ones of the plurality of memory cells therein and provide a second one of said bias signals to another one of

the plurality of memory arrays to enable erasing of said another one of the plurality of memory arrays while reading said one of the plurality of memory arrays.

104. The data storage system of claim 103 further comprising:

a plurality of local sense amplifiers, each of said plurality of local sense amplifiers being coupled to a corresponding memory array and coupled through bit lines to memory cells in said corresponding memory array; and

a plurality of global sense amplifiers, each global sense amplifier being coupled to a group of said plurality of local sense amplifiers to generate an output signal indicative of the content of selected memory cells.

105. The data storage system of claim 104 wherein said at least one memory decoder selectively enabling two of said local sense amplifiers coupled to a corresponding global sense amplifier while selectively coupling an output of one of the local sense amplifiers to said corresponding global sense amplifier and enabling another one of said local sense amplifiers coupled to said corresponding global sense amplifier while selectively coupling an output of another one of said two local sense amplifiers.

106. The data storage system of claim 105 wherein each global sense amplifier is selectively coupled to a group of said local sense amplifiers to capacitively sense a voltage on said group of local sense amplifiers.

107. The data storage system of claim 104 wherein each global sense amplifier is selectively coupled to a group of said local sense amplifiers to capacitively sense a voltage on said group of local sense amplifiers.

108. The data storage system of claim 104 wherein each global sense amplifier auto zeros an input and output to zero out offset of the global sense amplifier.

109. A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, each memory cell is configurable to store one of 2^N values, where N is two or greater; and

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells, and provide a first one of said bias signals to one of the plurality of memory arrays to select ones of the plurality of memory cells therein and provide a second one of said bias signals to another one of the plurality of memory arrays to enable erasing of said another one of the plurality of memory arrays while erasing said one of the plurality of memory arrays.

110. The data storage system of claim 109 further comprising:

a plurality of local sense amplifiers, each of said plurality of local sense amplifiers being coupled to a corresponding memory array and coupled through bit lines to memory cells in said corresponding memory array; and

a plurality of global sense amplifiers, each global sense amplifier being coupled to a group of said plurality of local sense amplifiers to generate an output signal indicative of the content of selected memory cells.

111. The data storage system of claim 110 wherein said at least one memory decoder selectively enabling two of said local sense amplifiers coupled to a corresponding global sense amplifier while selectively coupling an output of one of the local sense amplifiers to said corresponding global sense amplifier and enabling another one of said local sense amplifiers coupled to said corresponding global sense amplifier while selectively coupling an output of another one of said two local sense amplifiers.

112. The data storage system of claim 111 wherein each global sense amplifier is selectively coupled to a group of said local sense amplifiers to capacitively sense a voltage on said group of local sense amplifiers.

113. The data storage system of claim 110 wherein each global sense amplifier is selectively coupled to a group of said local sense amplifiers to capacitively sense a voltage on said group of local sense amplifiers.

114. The data storage system of claim 110 wherein each global sense amplifier auto zeros an input and output to zero out offset of the global sense amplifier.

115. A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, each memory cell is configurable to store one of 2^N values, where N is two or greater; and

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells, and provide a first one of said bias signals to one of the plurality of memory arrays to select ones of the plurality of memory cells therein and provide a second one of said bias signals to another one of the plurality of memory arrays to enable writing of said another one of the plurality of memory arrays while writing said one of the plurality of memory arrays.

116. The data storage system of claim 115 further comprising:

a plurality of local sense amplifiers, each of said plurality of local sense amplifiers being coupled to a corresponding memory array and coupled through bit lines to memory cells in said corresponding memory array; and

a plurality of global sense amplifiers, each global sense amplifier being coupled to a group of said plurality of local sense amplifiers to generate an output signal indicative of the content of selected memory cells.

117. The data storage system of claim 116 wherein said at least one memory decoder selectively enabling two of said local sense amplifiers coupled to a corresponding global sense amplifier while selectively coupling an output of one of the local sense amplifiers to said corresponding global sense amplifier and enabling another one of said local sense amplifiers

coupled to said corresponding global sense amplifier while selectively coupling an output of another one of said two local sense amplifiers.

118. The data storage system of claim 117 wherein each global sense amplifier is selectively coupled to a group of said local sense amplifiers to capacitively sense a voltage on said group of local sense amplifiers.

119. The data storage system of claim 116 wherein each global sense amplifier is selectively coupled to a group of said local sense amplifiers to capacitively sense a voltage on said group of local sense amplifiers.

120. The data storage system of claim 116 wherein each global sense amplifier auto zeros an input and output to zero out offset of the global sense amplifier.

121. A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, each memory cell is configurable to store one of 2^N values, where N is two or greater; and

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells, and provide a first one of said bias signals to one of the plurality of memory arrays to select ones of the plurality of memory cells therein and provide a second one of said bias signals to another one of the plurality of memory arrays to enable erasing of said another one of the plurality of memory arrays while writing said one of the plurality of memory arrays.

122. The data storage system of claim 121 further comprising:

a plurality of local sense amplifiers, each of said plurality of local sense amplifiers being coupled to a corresponding memory array and coupled through bit lines to memory cells in said corresponding memory array; and

a plurality of global sense amplifiers, each global sense amplifier being coupled to a group of said plurality of local sense amplifiers to generate an output signal indicative of the content of selected memory cells.

123. The data storage system of claim 122 wherein said at least one memory decoder selectively enabling two of said local sense amplifiers coupled to a corresponding global sense amplifier while selectively coupling an output of one of the local sense amplifiers to said corresponding global sense amplifier and enabling another one of said local sense amplifiers coupled to said corresponding global sense amplifier while selectively coupling an output of another one of said two local sense amplifiers.

124. The data storage system of claim 123 wherein each global sense amplifier is selectively coupled to a group of said local sense amplifiers to capacitively sense a voltage on said group of local sense amplifiers.

125. The data storage system of claim 122 wherein each global sense amplifier is selectively coupled to a group of said local sense amplifiers to capacitively sense a voltage on said group of local sense amplifiers.

126. The data storage system of claim 122 wherein each global sense amplifier auto zeros an input and output to zero out offset of the global sense amplifier.